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ENERGY-EFFICIENT 4-bit FULL ADDER DESIGN USING MODIFIED GDI TECHNIQUE IN 130nm TECHNOLOGY USING MENTOR GRAPHICS SOFTWARE

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ABSTRACT
Addition is a fundamental arithmetic operation, essential for various digital circuits. High-performance adders are critical components of Arithmetic Logic Units (ALUs) in Integrated Circuits (ICs). This paper focuses on the design and analysis of 4-bit full adders (FAs) utilizing Gate-Diffusion Input (GDI) technology, an alternative to traditional Complementary Metal Oxide Semiconductor (CMOS) techniques. The objective is to evaluate the power consumption, propagation delay, and transistor count of GDI-based FAs. By comparing GDI-based FAs with CMOS-based counterparts, this research aims to identify potential advantages and trade-offs of GDI technology for low-power, high-performance IC design.

Keywords:
Integrated circuits (IC), arithmetic logical units (ALU), Complementary Metal Oxide Semiconductor (CMOS), gate-diffusion input (GDI), full adder(FA), Modified GDI (MGDI).

INTRODUCTION

Continuous pursuit of miniaturization and low-power operation in integrated circuits (ICs) has led to the exploration of novel device and circuit techniques. Gate-Diffusion Input (GDI) technology, an alternative to traditional CMOS, offers potential advantages in terms of reduced power consumption and improved performance. By leveraging the unique characteristics of GDI devices, it is possible to design energy-efficient circuits that meet the stringent requirements of modern electronic systems. This paper aims to reduce transistor count by utilizing full-swing GDI techniques, compared to conventional CMOS designs. A detailed analysis of design parameters, including transistor count, power consumption, propagation delay, and circuit complexity, will be undertaken.

Recent research has focused on developing energy-efficient full adder architectures using Gate-Diffusion Input (GDI) logic for arithmetic applications. GDI-based designs offer significant advantages in terms of power consumption, area, and delay compared to conventional CMOS approaches (Aggarwal & Garg, 2021; Bilal N Md et al., 2020). Full-swing GDI-based adders have been proposed to address low-swing and noise issues at low supply voltages, demonstrating improved signal integrity and driving capability (Aggarwal & Garg, 2021). These designs have shown power savings of up to 14.8% over hybrid designs and 55% reduction in area (Aggarwal & Garg, 2021). Performance analyses have revealed that GDI-based arithmetic circuits can achieve more than 41% improvement in delay and 32% in energy consumption compared to conventional CMOS full adders (Bilal N Md et al., 2020). The GDI technique allows for reduced transistor count and power consumption in digital circuit design, making it particularly suitable for embedded systems (Batta et al., 2012; Chandralekha et al., 2020).

Majid Amini-Valashani & S. Mirzakuchaki (2020) proposed two new MGDI-based full adders that achieve full-swing operation and demonstrate significant improvements in power consumption and power-delay product. Kumar et al., (2019) proposed a new hybrid 1-bit full adder circuit design that combines GDI logic and MVT transistors to achieve minimum energy consumption and small area, with simulation results showing >57% energy savings and 92% EDP savings compared to prior designs (Sanapala & Sakhtivel, 2019). The research introduced a hybrid full adder design combining GDI logic and multi-threshold voltage transistor logic, achieving substantial energy savings at ultra-low voltages. The paper presents two new low-power, energy-efficient full adder cell designs based on MGDI logic

that show 24-56% and 36-66% improvements in power consumption and power-delay product, respectively. Their design showed robustness against process variations and scalability to smaller technology nodes. Deepgandha Shete & Anuja Askhedkar (2021) compared full swing GDI and CMOS techniques for full adder design, noting that GDI offers better speed and lower complexity while maintaining low power consumption. These studies collectively demonstrate the potential of GDI and MGDI techniques in creating power-efficient, area-efficient, and high-performance full adder designs for modern computing systems.

According to Zain Z. (2019, April) his research CMOS first by doing The full adder which is constructed using a conventional CMOS topology and consists of 28 transistors. However, this high transistor count can result in increased power consumption and a larger usage of area per die. Regardless, the research was able to provide a full swing output, good noise resistance, and good ranges of operating temperatures. The author found that with a supply voltage of 1.8V and an ambient temperature of 27 degrees celsius, and considering that all PMOS and NMOS transistors have a minimum channel length (Lmin) of 180 nanometers, conducted a transient analysis over a 50-millisecond time span and examined the output voltage at various nodes. Findings from [4] revealed that the circuit exhibited power consumption within the range of 1084 nanowatts (minimum) to 1217 nanowatts (maximum). The range of propagation delay time was determined to be 22.6 ps (minimum) and 31.8 ps (maximum) range.

According to Dhavachelvan and Uma research article (December, 2012) it is inferred that the paper's primary focus is on introducing novel designs for primitive cells and presenting five distinct topologies for circuit-level implementations of full adders using the GDI (Gate Diffusion Input) technique. The modified GDI primitive cells are developed and their differences from conventional CMOS GDI cells are analyzed. While the GDI technique offers advantages like reduced power consumption, fewer transistors, and high speed, it also present complexities during the fabrication process thus implementing GDI techniques using twin-well CMOS or Silicon on Insulator (SOI) processes can elevate both the complexity and cost of fabrication.

Previous research has primarily focused on 1-bit Full Adder (FA) designs, achieving varying levels of full-swing output. Some studies have employed older and larger lithographic nodes, while others have opted for more complex designs requiring larger chip die areas. Despite these differences, all research efforts have successfully reduced transistor count, propagation delay, and power consumption for their respective FA designs. This project aims to further optimize GDI-based FA designs by minimizing transistor count, reducing propagation delay, lowering power consumption, and maximizing full-swing output. By simplifying the design and reducing chip die area, we seek to achieve a more efficient and effective FA implementation. This project aims to further optimize GDI-based FA designs by minimizing transistor count, reducing propagation delay, lowering power consumption, and maximizing full-swing output. By simplifying the design and reducing chip die area, we seek to achieve a more efficient and effective FA implementation.

METHODOLOGY

This paper outlines a methodology that involves Design flowchart. For the software component, Mentor Graphics with Pyxis will be utilized, employing the 130nm process technology provided by Siemens EDA. Primitive logic gates will be designed using GDI full-swing technology. A library of optimized gates will be created, selecting components based on their power consumption, propagation delay, transistor count, design complexity/area, and power-delay product (PDP). This optimized library will be used to design a 4-bit full adder, which will be analyzed and compared to a CMOS equivalent.

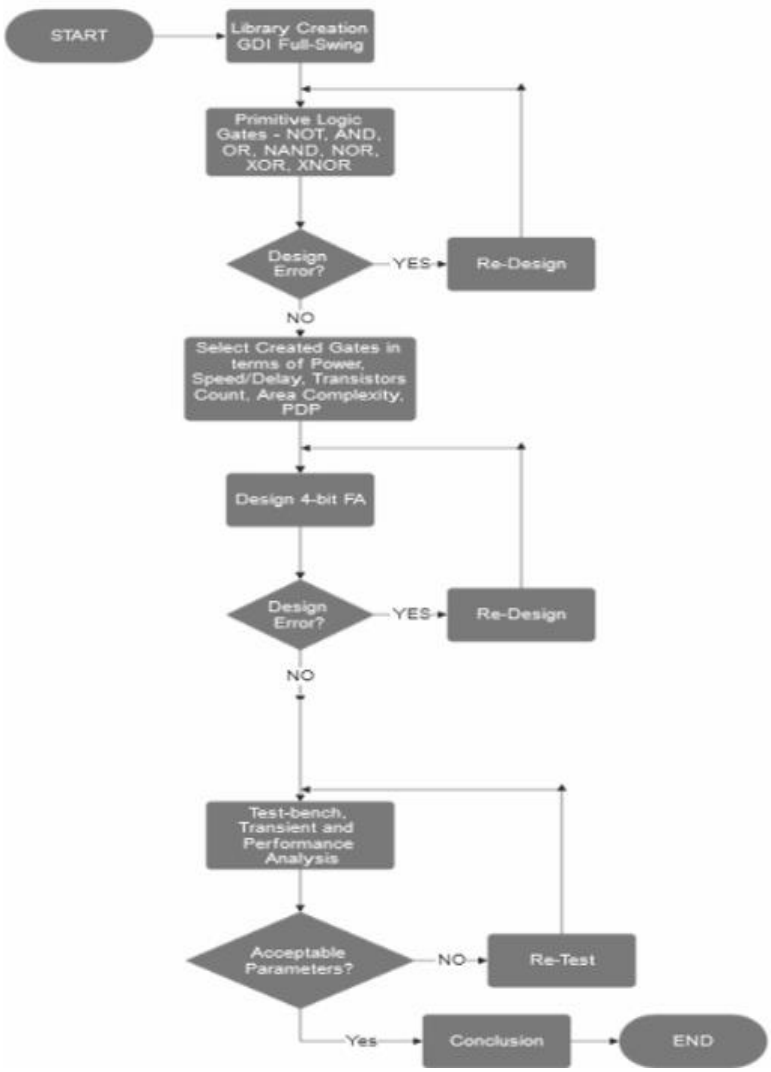

Figure 1: Design flowchart

Design Analysis

The designed FA with GDI technology using 130nm node process along with achieving full swing output will be analyzed in these following terms. The designed FA will be analyzed in terms of transistor count. A GDI cell consisting of the PMOS and NMOS can be designed in such a way that it will achieve n+2 inputs.

$$M=2*2n-1=2n-1+1=2*N=2n \quad (1)$$

$$N=2n-1 \quad (2)$$

Based on the equations (1) and (2) for GDI, where M is the maximal number of transistors that are needed to implement and N is the maximal count of GDI cells and n is the number of input variables. The technology used in this paper is 130 nm size, if we go for nm technology then the size (W/L) of the transistor needs to be changed based on the technology library. The lithographic process node size or the

technology node will also be compared. In the case of this project is a 130nm feature size which often refers to the Length from the W:L ratio or W/L. The designed FA will also be analyzed in terms of its wiring, area and circuitry design complexity. The analysis will be done in comparison to an equivalent CMOS FA and compared by inspections.

The designed GDI-based FA with full-swing output will also be analyzed in terms of its propagation delay. The propagation delay is related to the number of transistors along with its geometric complexity as in the wiring and thus it is determined by the input transition time also known as logical effort/time and also the load capacitance. The delay decreases with high input transition as in less logical effort or time for the output to go from a transient state into a steady-state. Propagation delay of MOSFETs can increase with increase in number of capacitance like load capacitance (fanouts or fan-outs) at the output voltage and the parasitic capacitances that exists at the diffusion terminals along with the wiring complexity which correlates with the area of the design. Thus for the propagation delay of the MOSFETs, it can be generalized with the following formula.

$$Transition\ Time = \frac{1}{Logical\ Effort} \quad (3)$$

$$Transistor\ Propagation\ Delay \propto \frac{Capacitances * Vdd * Vt * Resistance}{Transition\ Time * FrequencyClock} \quad (4)$$

$$RC = Resistance * Capacitance = Tau\ [s] \quad (5)$$

The designed FA will also be analyzed in terms of its power consumption or power dissipation. A high power usage will lead to more generation of heat energy as the acting usage of power would result in the reaction of high heat generation and thus an equal reaction of opposite power efficiency.

$$Static\ Power\ Usage = Vcc * Icc(op) \quad (6)$$

$$Dynamic\ (transient) Power\ Usage = Cpc * Vcc^2 * fclock * N \quad (7)$$

From the above formulas (6) and (7) are that the Vcc is the supply voltage, Icc is the supply current, fclock is the clock frequency while N is the number of transistors input switching. The FA will also be analyzed in terms of the PDP or Power Delay Product. The PDP is the product of the power consumption with the time delay and thus a lower power and/or lower delay can lead to lower PDP noted in equation (8).

$$PDP = Power\ Consumption\ [W] * Propagation\ Time\ Delay\ [s] \quad (8)$$

While not an industrial standard, the product of the entire transistor count along with the propagation delay can also be analyzed.

$$Tr * Delay = Transistor\ Count * Propagation\ Delay \quad (9)$$

The Rise Time (RS) is a measure of the pulses transitioning from Low (minimum) to High (maximum) while the Fall Time (FT) is a measure from High to Low states.

Design Modelling

The design techniques that are going to be checked in this research paper are CMOS and GDI. CMOS is the conventional type technology that is used in Industries. GDI is a technology that is developed to overcome the problems in existing CMOS. The modelling of the design for each digital circuit design techniques are different. This sub-section will discuss the expected design modelling for the CMOS and the GDI techniques.

CMOS Cell Predictive Steps:

- Complementary Boolean expression or equation for the design.
- Pull-Up Network (PMOS cell) – AND operator in parallel, OR operator in series.
- Pull-Down Network (NMOS cell) – AND operator in series, OR operator in parallel.
- Vdd to Pull-Up
- Vss or GROUND or GND to Pull-Down
- Inverter or NOT cell reserved for any complementary inputs.

While the GDI with full swing output cell steps are as predicted below.

- GDI with Full-Swing Output Cell Predictive Steps:
- Two transistors connected in series and the Gate input of both transistor will be fixed with an input. The source input of P-MOS will be P-diffusion The drain of N-MOS will be N-diffusion
- Doing a Karnaugh Mapping (K-Map) of 2x2 of PN/BCB, if P-diffusion = 00 then P to GND. If P = 01 then B to P. If P = 10 then BC to P. If P = 11 then P to VDD.
- If N-diffusion = 00 then N to GND. If N = 01 then B to N. If N = 10 then BC to N. If N = 11 then N to Vdd.
- In order to get complementary output, wherever the diffusion terminals are connected then either PMOS or NMOS will be connected in parallel to it depending on where the diffusion terminal is situated at either the Pull-Down Network or Pull-Up Network.

RESULTS & ANALYSIS

The comparisons of MOSFETs IC logic design using GDI, GDI Full Swing (GDI FS) and CMOS are presented in Table 1, until Table 9.

Table 1: GDI, GDI FS and CMOS for AND Gate

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	3p	2	12n
GDI Full Swing	230p	6	12n
CMOS	343p	6	60n

Table 2: GDI, GDI FS and CMOS for OR Gate

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	12.5p	2	10n
GDI Full Swing	480p	6	10n
CMOS	561p	6	20n

Table 3: GDI, GDI FS and CMOS for NAND Gate

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	184p	4	10n
GDI Full Swing	186p	5	10n
CMOS	188p	4	22n

Table 4: GDI, GDI FS and CMOS for NOR Gate

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	324p	4	20n
GDI Full Swing	408p	5	20n
CMOS	342p	4	21n

Table 5: GDI, GDI FS and CMOS for XOR Gate

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	170p	4	20n
GDI Full Swing	640p	8	20n
CMOS	1111p	8	22n

Table 6: GDI, GDI FS and CMOS for XNOR Gate

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	320p	4	10n
GDI Full Swing	585p	8	10n
CMOS	891p	8	21n

Based on observation from Table 1 to 6, power dissipation and number of transistors for logic gates designed using GDI is lower than GDI full swing. Meanwhile the propagation delay for both GDI and GDI full swing design shows the same performance.

Table 7: GDI, GDI FS and CMOS for Half Adder

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	-	-	-
GDI Full Swing	2200p	14	10n
CMOS	3000p	14	21n

Table 8: GDI, GDI FS and CMOS for Full Adder

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	-	-	-
GDI Full Swing	2800p	34	11n
CMOS	3500p	34	20n

Table 9: GDI, GDI FS and CMOS for 4-bit Full Adder

	Power Dissipation (W)	Number of Transistors	Propagation Delay fall to fall time (s)
GDI	-	-	-
GDI Full Swing	9000p	136	11n
CMOS	15000p	136	26n

DISCUSSION

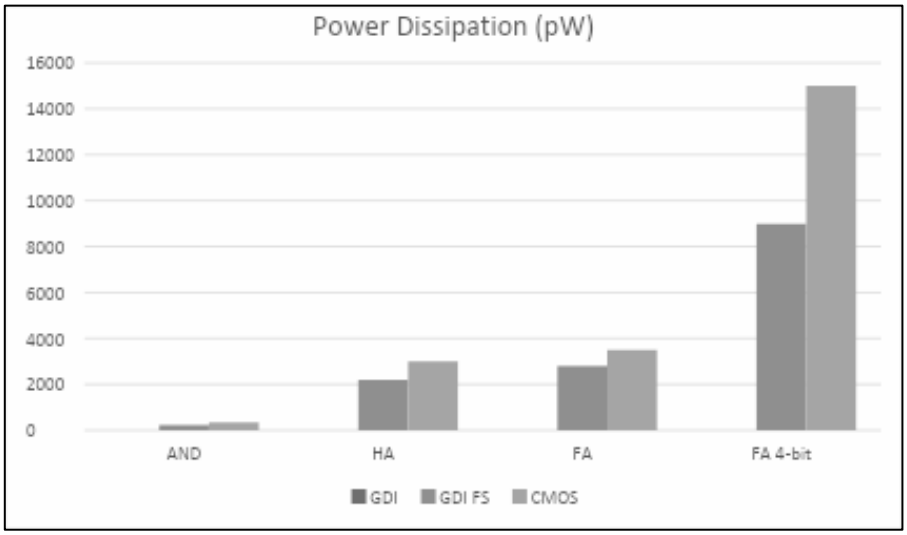

Figure 2 Power Dissipation Comparison

Based on the obtained results from the designed IC logic circuits, utilizing the 130nm MOSFET lithographic process and employing GDI logic, GDI FS logic, and CMOS logic, show that GDI logic achieves the lowest delay and power dissipation, resulting in the least heat generation over time. This is primarily due to the reduced number of MOSFETs in GDI logic, which minimizes propagation pathways and parasitic capacitances, leading to lower power consumption and heat output compared to the other two logic types.

However, this energy efficiency comes at the cost of switching speed. While GDI logic is slower than CMOS, it offers improved scalability due to its lower propagation delay. This advantage is particularly evident when comparing GDI FS logic to CMOS with an equal transistor count. GDI FS logic, despite using the same number of transistors as CMOS, theoretically achieves lower propagation delay and power usage while maintaining comparable speed at the same lithographic node. However, issues arise with simultaneous input/output transitions (rise and fall times), which can cause fluctuations in output, affecting stability.

Additionally, GDI and GDI FS logic face challenges with full-swing output. In GDI, inputs are applied to the gates and sources, while VDD and VSS are tied to the bulk substrates. This design leads to output voltage spikes or fluctuations, in contrast to the ideal full-swing outputs seen in CMOS logic. Potential solutions to mitigate this issue include implementing buffers with comparators or triggers, or reducing internal parasitic capacitances. Another option could involve using alternative semiconductor materials, such as Gallium Arsenide (GaAs), to improve performance and reduce parasitic effects. Finally

the Modified GDI has fewer transistor count and less power dissipation met our goal of this research. The result analysis shows better performance when compared with CMOS.

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